M5M4V16169TP-10,-12,-15,-20

16MCDRAM:16M(1024K-WORD BY 16-BIT) CACHED DRAM WITH 16K (1024-WORD BY 16-BIT) SRAM

Preliminary

This document is a preliminary Target Spec. and some of the contents are subject to change without notice.

DESCRIPTION

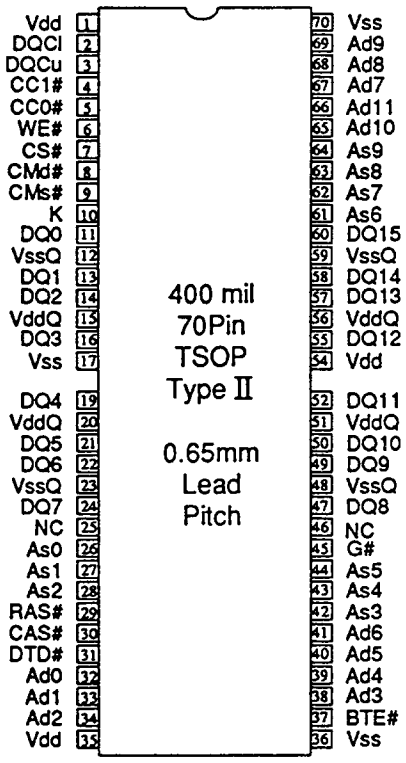
1. The M5M4V16169TP is a 16M-bit Cached DRAM which integrates input registers, a 1,048,576-word by 16-bit dynamic memory array and a 1024- word by 16-bit static RAM array as a Cache memory (block size 8x16) onto a single monolithic circuit. The block data transfer between the DRAM and the data transfer buffers (RB1/RB2/WB1/WB2) is performed in one instruction cycle, a fundamental advantage over a conventional DRAM/SRAM cache.
2. The RAM is fabricated with a high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low cost are essential. The use of quadruple-layer polysilicon process combined with silicide and double layer aluminum wiring technology, a single-transistor dynamic storage stacked capacitor cell, and a six-transistor static storage cache cell provide high circuit density at reduced costs.

FEATURES

Type name	SRAM Access/cycle	DRAM Access/cycle	Power Dissipation (Typ)
M5M4V16169TP-10	10ns/10ns	60ns/120ns	DRAM: 380mW SRAM: 860mW
M5M4V16169TP-12	12ns/12ns	60ns/120ns	DRAM: 320mW SRAM: 800mW
M5M4V16169TP-15	15ns/15ns	70ns/130ns	DRAM: 270mW SRAM: 710mW
M5M4V16169TP-20	20ns/20ns	70ns/130ns	DRAM: 230mW SRAM: 540mW

- 70-pin,400-mil TSOP (typeⅢ) with 0.65mm lead pitch and 23.49mm package length.
- Multiplexed DRAM address inputs for reduced pin count and higher system densities.
- Selectable output operation (transparent / latched / registered) using set command register cycle.
- Single 3.3V +/- 0.3V Power Supply.
- 4096 refresh cycles every 64ms (Ad0->Ad11).
- Programmable burst length (1,2,4,8) and burst sequence (sequential, interleave) with no latency.
- Applicable for both direct-mapped and associative systems.
- Synchronous design for precise control with an external clock (K).
- Output retention by advanced mask clock (CMs#).
- All inputs/outputs low capacitance and LVTTL compatible.
- Asynchronous output enable (G#) for bus control.
- Separate DRAM and SRAM address inputs for fast SRAM access.
- Page Mode capability.
- Auto Refresh capability.
- Self Refresh capability.

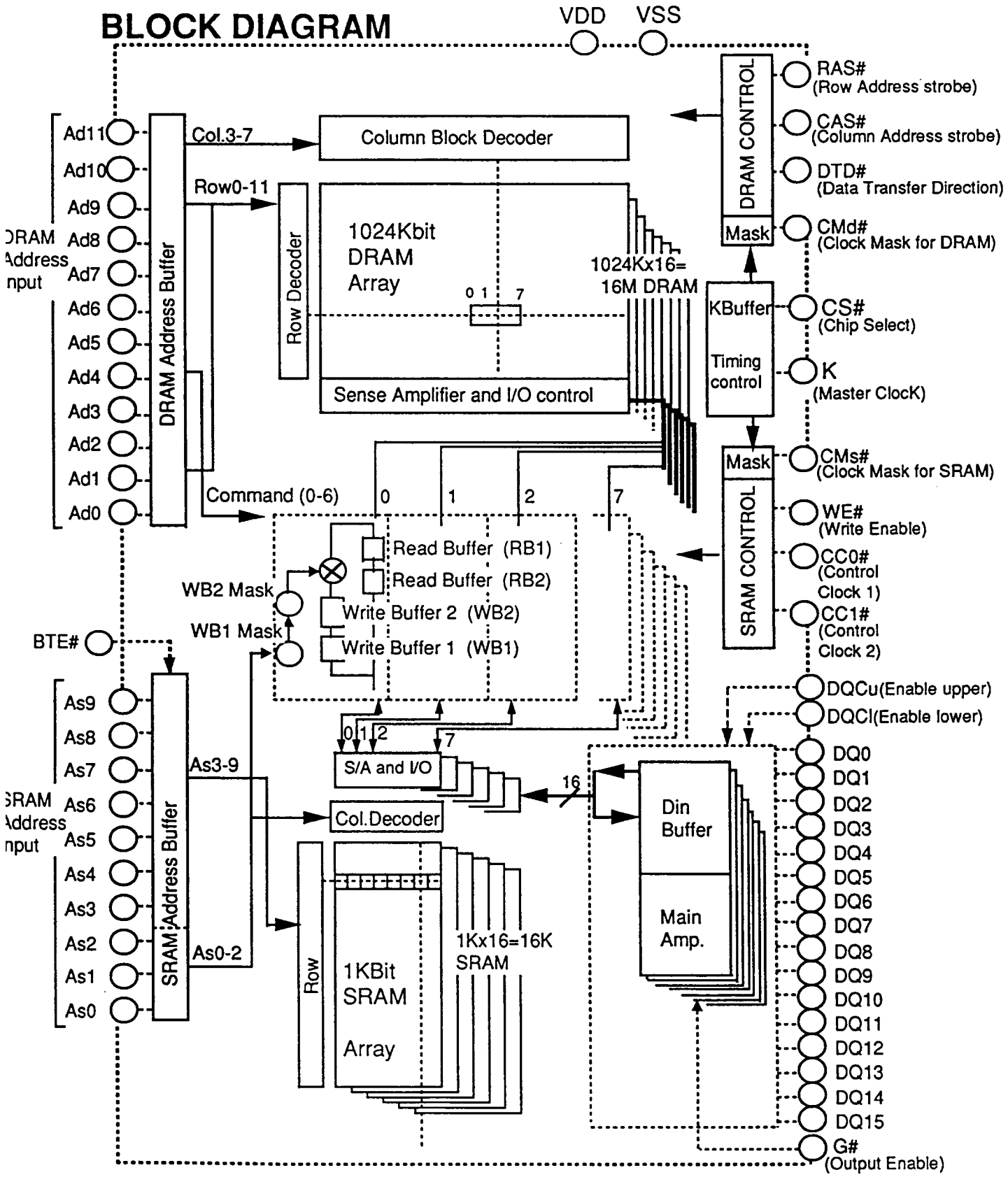
PIN CONFIGURATION (TOP VIEW)



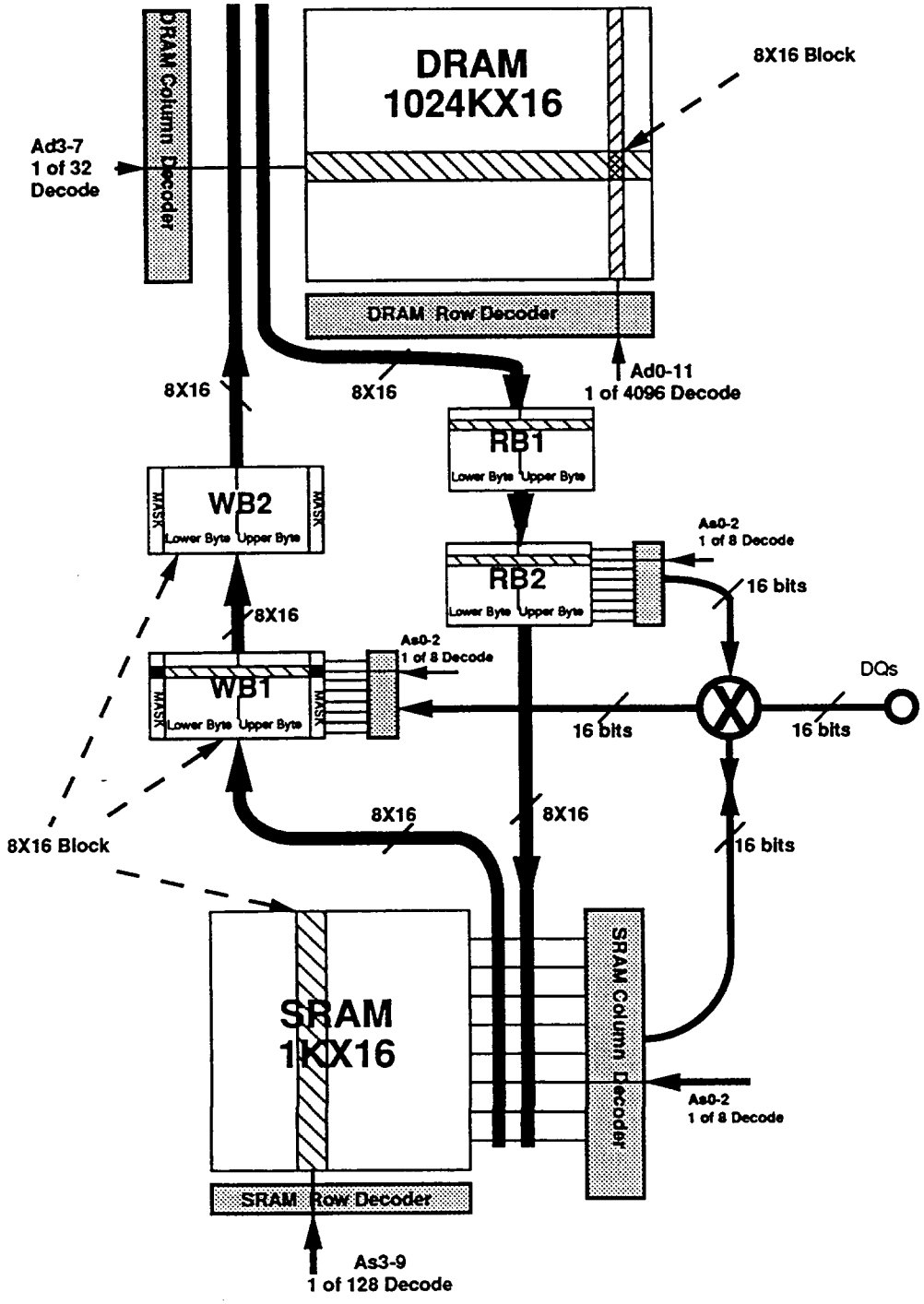
Package code:70P3S

K	: Master Clock
CS#	: Chip Select
CMd#	: DRAM Clock Mask
RAS#	: Row Addr. Strobe
CAS#	: Column Addr. Strobe
DTD#	: Data Transfer Direction
Ad	: DRAM Address
CMs#	: SRAM Clock Mask
CC0#,CC1#	: Control Clocks
WE#	: Write Enable
DQC(u/l)	: I/O Byte Control
As	: SRAM Address
G#	: Output Enable
BTE#	: Burst Enable
DQ	: Data I/O
Vdd	: Power Supply
VddQ	: DQ Power Supply
Vss	: Ground
VssQ	: DQ Ground

BLOCK DIAGRAM



BLOCK DIAGRAM #2



FUNCTION TRUTH TABLE

Mnemonic CODE	CS#	SRAM					As (SRAM address)	DRAM				Ad (DRAM address)			
		Previous CMs#	CC0#	CC1#	DQC (u/l)	WE#	As0-9	Previous CMd#	RAS#	CAS#	DTD#	Ad0-11	Ad2	Ad1	Ad0
NOP	H	H	X	X	X	X	X	H	X	X	X	X			
SPD	X	L	X	X	X	X	X	X	X	X	X	X			
DES	L	H	H	H	X	X	X	X	X	X	X	X			
SR (10)	L	H	H	L	H/L (11)	H	As0-9	X	X	X	X	X			
SW (10)	L	H	H	L	H/L (11)	L	As0-9	X	X	X	X	X			
BRT	L	H	L	H	L	H	As3-9	X	X	X	X	X			
BWT	L	H	L	H	L	L	As3-9	X	X	X	X	X			
BRTR (10)	L	H	L	H	H/L (11)	H	As0-9	X	X	X	X	X			
BWTW (10)	L	H	L	H	H/L (11)	L	As0-9	X	X	X	X	X			
BR (10)	L	H	L	L	H/L (11)	H	As0-2 (2)	X	X	X	X	X			
BW (10)	L	H	L	L	H/L (11)	L	As0-2 (2)	X	X	X	X	X			
DPD	X	X	X	X	X	X	X	L	X (1)	X (1)	X (1)	X			
DNOP	L	X	X	X	X	X	X	H	H	H	X	X			
DRT	L	X	X	X	X	X	X	H	H	L	H	Ad3-7 (2) (Col.Block)	0	0	0
DWT1	L	X	X	X	X	X	X	H	H	L	L	Ad3-7 (2) (Col.Block)	0	0	0
DWT1R	L	X	X	X	X	X	X	H	H	L	L	Ad3-7 (2) (Col.Block)	0	0	1
DWT2	L	X	X	X	X	X	X	H	H	L	L	Ad3-7 (2) (Col.Block)	0	1	0
DWT2R	L	X	X	X	X	X	X	H	H	L	L	Ad3-7 (2) (Col.Block)	0	1	1
ACT	L	X	X	X	X	X	X	H (9)	L	H	H	Ad0-11 (Row Add.)			
PCG	L	X	X	X	X	X	X	H	L	H	L	X			
ARF	L	X	X	X	X	X	X	H (7)	L	L	H	X			
SRF	L	X	X	X	X	X	X	H (8)	L	L	H	X			
SCR	L	X	X	X	X	X	X	H	L	L	L	Command			

NOTES
1) For the DPD function, the RAS#, CAS# and DTD# inputs are DON'T CARE except for the L,L,H combination (Respectively).
2) The unused addresses must be set to Low.
3) Use New: If BW or BWT or BWTW is initiated the same cycle as DWT1 or DWT1R, new data is loaded into the buffer and transferred to DRAM.
4) Clear 1 or 2 Transfer Mask Bits (as addressed by As0-2 and DQCU/L).
5) Actual number of bits transfer depends on the state of the DTBW Mask and the DQCU/DQCL inputs.
Note: If DQC(U/L) is Low, the corresponding DQ(s) is(are) disabled (Input and Output Buffer). SR,SW,BR and BW cycles with DQCU and DQCL Low result in a Deselect SRAM operation.
6) Following a DWT1 or DWT1R cycle, the entire WB1 Transfer Mask is Set (i.e. , data can no longer be transferred from WB1 to DRAM. Succeeding Buffer-Writes or Buffer Write Transfers will Clear Mask bits.
7) CMd# during current cycle must be High (see timing diagram for Auto-Refresh).
8) CMd# during current cycle must be Low (see timing diagram for Self-Refresh).
9) A RAS only refresh can be accomplished by issuing an ACT followed by PCG. (tRC must be observed)
10) These functions can be used with Burst Mode.
11) When DQCU is Low, DQ 15-8 are in a high Z state. When DQCL is Low DQ 7-0 are in a high Z state. See DQCU/L Pin Description for more detail.

Detail of Write Buffer Transfer Masks:

Write Buffer 1 (WB1) and Write Buffer 2 (WB2) both have a transfer mask associated with them. These masks when "cleared" will allow data that has been written to WB1 to pass to WB2, and from WB2 to the DRAM. When the mask is "set" the data in the WB1 is not allowed to be transferred to WB2, or from WB2 to the DRAM.

Write Buffer 1 mask:
The transfer mask has two masking operations associated with each of the eight words(16 bit) of data that can be written to the buffer. DQCU and DQCL are used to mask the I/O while writing to WB1. The corresponding mask bit is set for the 8-bits not being written and cleared for those that are being written. If DQCU/L are not used to mask the I/O during a buffer write both bits associated with the buffer write address are cleared. The mask bits that are cleared will allow the data written to their corresponding address to pass to the WB2 during a DWT1 or a DWT1R. At the same time the data is transferred, the contents of WB1 mask is transferred to the WB2 mask.

The mask associated with WB1 is cleared during a buffer write (BW), buffer write transfer (BWT), or buffer write transfer write (BWTW). The mask is set with a dram write transfer1 (DWT1), dram write transfer1 read (DWT1R), or an SCR with Ad(0) = H. (See timing diagram below.)

Write Buffer 2 mask:
The WB2 mask data is supplied from the state of the WB1 mask when a DWT1 or a DWT1R occurs. The mask data from the WB1 is held in the WB2 mask until another DWT or DWT1R occurs. If a bit is set in the WB2 mask the data will not be transferred to the DRAM. If the bit is cleared the data will be allowed to transfer to the DRAM.